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	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L69	L68 and (trap$3 or exception$1 or interrupt$3)	6
☐	L68	(6081890 or 5596755 or 6385718 or 6272453 or 6917997 or 5701493 or 5721931).pn.	7
☐	L67	L32 and L2	3
☐	L66	firmware and L64	112
☐	L65	L2 and L64	1
☐	L64	L24 same (L25 or L26)	630
☐	L63	L62 not L58	20
☐	L62	(L55 or L56) and L61	22
☐	L61	(710/260 |710/261 |710/262 |710/263 |710/264 |710/265 |710/266 |710/267 |710/268 |710/269).ccls.	1932
☐	L60	(712/260).ccls.	0
☐	L59	(712/260 |712/261 |712/262 |712/263 |712/264 |712/265 |712/266 |712/267 |712/268 |712/269).ccls.	0
☐	L58	(L55 or L56) and L57	16
☐	L57	(712/244).ccls.	545
☐	L56	(712/229).ccls.	314
☐	L55	(712/43).ccls.	219
☐	L54	6041402.pn.	1
☐	L53	L49 and (interrupt$1 or exception$1 or trap$1)	16
☐	L52	6081890.pn.	1
☐	L51	6272453.pn.	1
☐	L50	6272453.uref.	4
☐	L49	6081890.uref.	26
☐	L48	legacy with L47	8
☐	L47	native with (interrupt$1 or exception$1 or trap$1)	993
☐	L46	multiplexing interrupts	3
☐	L45	native with legacy with (trap$3 or exception$1 or interrupt$3)	8
☐	L44	5608886.pn.	1
☐	L43	dual architecture exception$1	2
☐	L42	L41 and (interrupt$3 or exception$1 or trap$4)	5

	DB=USPT,PGPB; PLUR=NO; OP=ADJ		
☐	L41	('5598546'| '5638525'| '5774686'| '5781750'| '5930490')![pn]	5
	DB=PGPB,USPT; PLUR=NO; OP=ADJ		
☐	L40	non-native mode	35
☐	L39	(ia-32 with interrupt$3) and (ia-64 with interrupt$3)	5
☐	L38	interrupt$3 and L37	121
☐	L37	ia-32 and ia-64	434
☐	L36	merced and ia-32	13
☐	L35	native same L34	18
☐	L34	x86 with interrupt$1	227
☐	L33	x86 interrupt$1	30
☐	L32	(L29 or L30) same L31	147
☐	L31	16 bit$1 with interrupt$1	1232
☐	L30	32 bit$1 with interrupt$1	751
☐	L29	64 bit$1 with interrupt$1	224
☐	L28	interrupt$1 and L27	28
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☐	L26	64 bit$1 with microprocessor$1	987
☐	L25	32 bit$1 with microprocessor$1	3353
☐	L24	16 bit$1 with microprocessor$1	3413
☐	L23	interrupt$1 and L22	29
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☐	L21	32 bit$1 with processor$1	7518
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☐	L19	64 bit$1 with processor$1	2997
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☐	L16	32 bit$1 with processor	6807
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☐	L14	16-bit$1 with coprocessor$1	119
☐	L13	4349873.pn.	1
☐	L12	interrupt$1 and L7	12
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☐	L9	32-bit processor$1	868
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☐	L3	hardware interrupt$1 same L1	12
☐	L2	interrupt$1 same L1	100
☐	L1	real mode$1 same protected mode$1	562

END OF SEARCH HISTORY

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Giuseppe Desoli, Nikolay Mateev, Evelyn Duesterwald, Paolo Faraboschi, Joseph A. Fisher
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references, citings, index terms
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The Dynamic Execution Layer Interface (DELI) offers the following unique capability: it provides fine-grain control over the execution of programs, by allowing its clients to observe and optionally manipulate every single instruction---at run time---just before it runs. DELI accomplishes this by opening up an interface to the layer between the execution of software and hardware. To avoid the slowdown, DELI caches a private copy of the executed code and always runs out of its own private cache.In ...

2 The Flux OSKit: a substrate for kernel and language research
Bryan Ford, Godmar Back, Greg Benson, Jay Lepreau, Albert Lin, Olin Shivers
October 1997 **ACM SIGOPS Operating Systems Review , Proceedings of the sixteenth ACM symposium on Operating systems principles SOSP '97**, Volume 31 Issue 5
Publisher: ACM Press
Full text available: pdf(2.47 MB) Additional Information: full citation, references, citings, index terms

3 Porting RTOS device drivers to embedded Linux
Bill Weinberg
October 2004 **Linux Journal**, Volume 2004 Issue 126
Publisher: Specialized Systems Consultants, Inc.
Full text available: html(22.60 KB) Additional Information: full citation, abstract

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